REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed December 20, 2005. Claims 1-37 were pending in the present application. The present response amends claims 1-4, 6-8, 12, 19, 21, 23-26, and 29; and cancels claims 5, 20, 22, 28, and 31-37; leaving pending in the application claims 1-4, 6-19, 21, 23-27, and 29-30. Reconsideration of the rejected claims is respectfully requested.

I. Rejection under 35 U.S.C. §102

It is respectfully submitted that the rejections of the claims contained in the Office Action are somewhat unclear. The Office Action states on page 2 that claims 1-37 are rejected under 35 U.S.C. §102(b) as being anticipated by *Wahlstrom* (US 6,335,896), and that claims 12-37 are rejected under 35 U.S.C. §102(b) as being anticipated by *Sasaki* (US 4,768,172). In the arguments, however, *Wahlstrom* is only discussed with respect to claims 1-11, and *Sasaki* is only discussed with respect to claim 12.

Claims 13-18 appear to be rejected as discussed with respect to claims 2-11, which were rejected as being anticipated by *Wahlstrom* but depend from a claim discussed as being anticipated by *Sasaki*. Claims 19-32 are rejected without specific discussion of either reference, and there is no discussion of the reason for rejecting claims 33-37.

In order to further prosecution of the pending claims, Applicants will discuss claims 1-37 with respect to *Wahlstrom* and claims 12-37 with respect to *Sasaki*. Applicants respectfully request that if the present Amendment does not place the claims in condition for allowance, that any subsequent actions specifically point out where the elements recited in each claim are disclosed by the cited references.

(a) *Wahlstrom*

It is respectfully submitted that *Wahlstrom* does not disclose or suggest each element recited in claims 1-37. For instance, Applicants' claim 1 as amended recites an integrated circuit comprising an array of DRAM cells, each DRAM cell comprising:

> a first transistor having a gate coupled to a read word line and a drain coupled to a read bit line;

a second transistor coupled in series between the first transistor and a power supply voltage;

a third transistor coupled between the gate of the second transistor and a write bit line, a gate of the third transistor being coupled to a write word line;

a capacitor coupled to a gate of the second transistor; and

a pass gate coupled to the gate of the second transistor and the capacitor, wherein the write word line is not directly connected to the read word line, and wherein a voltage stored on the capacitor directly drives a gate voltage of the pass gate

(*emphasis added*). Such limitations are not disclosed by *Wahlstrom*.

Wahlstrom discloses a memory data storage system wherein pass transistors are used to separate short bit line segments (col. 1, lines 43-55). As seen, for example, in FIG. 15 of *Wahlstrom*, the pass gates are driven by a coupling voltage, and are not driven by a voltage stored on a capacitor coupled to a gate of a second transistor in a DRAM cell as recited by Applicants' claim 1. Applicants' claim 8 recites a CMOS inverter having an input coupled to the gate of the second transistor, wherein an output of the CMOS inverter drives a pass gate that programmably couples interconnect lines on the programmable integrated circuit. Relying instead on a coupling voltage to drive the pass gates, *Wahlstrom* similarly does not disclose such a limitation. Applicants' claim 12 recites a single inverter having an output coupled to a source of the first transistor in a DRAM cell. *Wahlstrom* does not disclose such a limitation. The remaining independent claims recite similar limitations to those discussed above, which are not disclosed by *Wahlstrom*. As such, *Wahlstrom* cannot anticipate pending claims 1-4, 6-19, 21, 23-27, and 29-30.

(b) *Sasaki*

Sasaki discloses a three-port memory cell including a bi-stable circuit comprised of a pair of inverter circuits having "their input-output terminals mutually connected" (col. 3, lines 33-59). *Sasaki* does not disclose a single inverter having an output coupled to a source of the first transistor in a DRAM cell as recited in Applicants' claim 12. Applicants' independent claims 19 and 26 recite directly driving a gate voltage of a pass gate using the charge stored on the capacitor, as discussed above, which is not disclosed by *Sasaki*. As such, *Sasaki* cannot anticipate pending claims 12-19, 21, 23-27, and 29-30.

Applicants therefore respectfully request that the rejection with respect to pending claims 1-4, 6-19, 21, 23-27, and 29-30 be withdrawn.

II. Amendment to the Claims

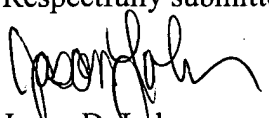
Unless otherwise specified, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the specification and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



Jason D. Lohr
Reg. No. 48,163

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
JDL:asb
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